

WHAT IS CLAIMED IS:

1. A semiconductor memory device having a shift redundancy function, the device comprising:

an address input circuit for receiving an address signal  
5 input;

a drive circuit for driving a memory array in compliance with the address signal;

a signal line for connecting the address input circuit and the drive circuit;

10 a redundant circuit located near the drive circuit for substituting other lines including a redundant line for a defective line in the memory array;

a defective line information store circuit for storing information showing the defective line; and

15 a supply circuit for supplying information stored in the defective line information store circuit to the redundant circuit via the signal line.

2. The semiconductor memory device according to claim  
20 1, wherein the supply circuit supplies information showing the defective line to the redundant circuit via the signal line when the semiconductor memory device is started.

3. The semiconductor memory device according to claim  
25 2, wherein the redundant circuit includes a storage circuit for storing the information.

4. A semiconductor memory device with a plurality of subblocks each including a drive circuit and a memory array, the device comprising:

5 a defective line information store circuit for storing information showing defective lines in the plurality of subblocks according to subblocks; and

a redundant circuit for substituting other lines including a redundant line for a defective line in each of the plurality of subblocks on the basis of information stored in  
10 the defective line information store circuit.

5. The semiconductor memory device according to claim 4, wherein the defective line information store circuit is shared by a plurality of subblocks.

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6. The semiconductor memory device according to claim 5, wherein the plurality of subblocks which share the defective line information store circuit are located in the direction perpendicular to the line.

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7. The semiconductor memory device according to claim 5, wherein each of the plurality of subblocks is divided into a plurality of sections, further wherein the redundant circuit performs a redundant process in each of the plurality of sections.

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8. The semiconductor memory device according to claim 4, wherein the defective line information store circuit is

located very near to a side of one of the plurality of subblocks parallel to the defective line.

9. The semiconductor memory device according to claim  
5 4, wherein the redundant circuit is located near to one of the plurality of subblocks, the device further comprising:

an address input circuit for receiving an address signal input;

a drive circuit for driving the plurality of subblocks  
10 in compliance with the address signal;

a signal line for connecting the address input circuit and the drive circuit; and

a supply circuit for supplying information stored in the defective line information store circuit to the redundant  
15 circuit via the signal line.

10. The semiconductor memory device according to claim 9, wherein the drive circuit is located along a side of one of the plurality of subblocks, further wherein the signal line is  
20 located parallel to the drive circuit.